(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

NEW GROUND(S) OF REJECTION

In the Final Rejection, claims 29-30 were grouped in the first rejection under 35 USC 103 based upon Doan et al. in view of Takeuchi and further in view of Maex et al. However, it was noted that the rejection of claims 29-30 should properly have been rejected along with their independent claims 19 and 23 which were rejected under Doan et al. in view of Takeuchi in view of Maex et al and further in view of Catabay et al., Jaiswal et al. and Hill et al. This is the only new ground of rejection present in the case with the remainder of the claims rejected as detailed in the Final Rejection.

Claims **1**, 5-6 and **12**, 16-17, 27-28 and **31** (NOTE: rejection of claims 29-30 have been removed from this ground of rejection and rejected in the next ground of rejection below) are rejected under 35 U.S.C. 103(a) as being unpatentable over Doan et al. US 5,196,360 in combination with Takeuchi US 5,766,997 and Maex et al. US Pub. 2002/0151170 A1.

*Re claims **1** and **12***, the Doan et al. reference discloses a method for fabricating a semiconductor device, figs 1-4, comprising:

forming a field region on a substrate 12 to define an active region; forming a gate pattern 22/14 on the active region, wherein the gate pattern includes sidewalls; forming spacers 24 on the sidewalls of the gate pattern; forming source/drain regions 16/18 aligned with the spacers on both sides of the gate pattern;

forming a metal film of *titanium* layer 28 for silicide on the entire surface of the substrate;

forming an N-rich titanium nitride layer 30 on the *titanium* layer, col. 4, lines 42-54;

thermally treating the *titanium* layer 28 for silicide and the N-rich titanium layer 30 to form a *titanium* silicide layer on the gate pattern and the source/ drain region, col. 4, line 55 to col. 5, line 8; and

selectively removing the *titanium* layer for silicide and the N-rich titanium nitride layer, wherein a top portion of the *titanium* silicide on the gate pattern and the source/drain region is exposed, col. 5, lines 17-21.

The Doan et al. reference uses a *titanium* layer 28 for silicide on the silicon substrate, it does not use Ni-based metal layer comprised of a nickel alloy for silicide on the silicon substrate. The Doan et al. reference *also* does not disclose cleaning the substrate using a wet cleaning process.

The Takeuchi reference discloses a method for fabricating a semiconductor device, embodiment 4, comprising:

forming a field region on a substrate 121 to define an active region, fig. 12A;

forming a gate pattern 125 on the active region, wherein the gate pattern includes sidewalls, fig. 12B;

forming spacers 130/131 on the sidewalls of the gate pattern, fig. 12D;

forming source/drain regions 127/128, 132/133 aligned with the spacers on both sides of the gate pattern;

"the source region is damaged by ion implantation. Before the silicide layer is formed, therefore, dilute HF cleaning is generally performed to expose the surface of the silicon substrate", col. 9, lines 35-37;

forming nickel **or** *titanium* **or** *cobalt* interchangeably, col. 1's lines 29-30, for a metal layer 136 for silicide on the entire surface of the substrate, **or** a nickel alloy, col. 7's lines 30-37:

a metal which can form silicide when reacted with silicon (this metal will be hereinafter called "silicide forming metal"). This silicide forming metal is, for example, refractory metal, more specifically, **at least one kind of metal selected from a group of** tungsten (W), *cobalt* (Co), *titanium* (Ti) ***and*** **nickel** (Ni). The first metal can be formed by a known thin film forming technology, such as sputtering or CVD.

forming a titanium nitride layer 137 on the Ni-based metal layer 136;

Then, a reaction suppressing layer is formed on the first metal layer including at least above the drain region and excluding above the source region. …

The reaction suppressing layer is formed of a material which causes no silicidation with silicon, or low-resistance material which may cause a silicidation but has a lower reactivity than the mentioned metal. One example of the material for the reaction suppressing layer is a metal nitride. This metal nitride may be a nitride of the aforementioned silicide forming metal. More specifically, the metal nitride is at least one kind selected from a group of titanium nitride, cobalt nitride, nickel nitride and tungsten nitride. When the reaction suppressing layer is formed of a metal nitride, this metal nitride should not necessarily be a nitride of the same metal as is used for the first metal layer. When a metal nitride is the material for the reaction suppressing layer, this layer may be formed by CVD, sputtering and the other applicable to this process, col. 7, lines 42-62.

thermally treating the Ni-based metal layer *comprised of nickel alloy* for silicide and the titanium nitride layer to form a nickel silicide layer on the gate pattern and the source/drain region, col. 17, lines 24-30; and

selectively removing the Ni-based metal layer for silicide and the titanium nitride layer, wherein a top portion of the nickel silicide on the gate pattern and the source/drain region is exposed, col. 17, lines 39-41.

The Takeuchi reference uses titanium nitride and makes the titanium nitride layer enriched with nitrogen while annealing "under the nitrogen or ammonia environment", col. 8, lines 12-13, it does not directly use N-rich titanium nitride.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the titanium layer for silicide of the Doan et al. reference with material of nickel or nickel alloy as taught by Takeuchi because: firstly, the titanium or nickel or nickel alloy layer for silicide are recognized as equivalent materials by Takeuchi; secondly, those materials as stated by Takeuchi would provide the metal layer for silicide of Doan et al. the same characteristic as analyzed by Takeuchi to enhance the reduction in sheet resistance (Takeuchi's col. 1, lines 24 and 65). Further, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the process of Doan et al. with the step of cleaning the substrate using a wet cleaning process as taught by Takeuchi as the cleaning step would mitigate implantation damage on exposed surface of the silicon substrate.

Alternatively, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of Takeuchi with N-rich titanium nitride of Doan because the N-rich titanium nitride of Doan would provide the titanium nitride of Takeuchi with inhibition ability of "outgrowth of silicide and potential short circuit paths between adjacent silicide contact areas" (Doan's abstract).

The combination of Doan et al. and Takeuchi teaches substantially all of the instant steps of fabricating a semiconductor device. The combination does not disclose the nickel alloy layer includes greater than 0 to about 20 % of one of the materials of Ta,

Zr, Hf, Pt, Pd, V, Nb or any combination of these (excluding Ti, Co and W, *re claims 27-28 and* ***31***).

The Maex et al. reference discloses these materials as elements in a Ni alloy used to formed Ni silicide [0014] or [0019], e.g. especially [0014] discloses

> The first layer structure can also include a cobalt-nickel alloy with the nickel content varying from 0 to 100%; … Also, other metals such as Pt or Pd can be chosen as elements that are present in the first layer structure…. or the elements Pt and Pd can be added in minor amounts to the first layer structure. Also, other elements such as Au, Ir, Os, Rh, Ti, Ta, W, Mo, Cr, C, and Ge can be part of the first layer structure.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of the combination with Maex et al.'s Ni alloy containing one of Ta, Zr, Hf, Pt, Pd, V, Nb or any combination of these materials, because the Ni alloy of Maex et al. would provide the combination with materials that "can withstand thermal treatment without significant degradation" [0009].

In this combination, choice of ratio of elements in the Ni-based metal layer would have been a matter of routine optimization because elements ratio, amongst many other variable parameters, is known to affect device properties and would depend on the desired device density on the finished wafer and the desired device characteristics. One of ordinary skill in the art would have been led to the recited greater than zero to 20 % of the chosen elements in the alloy through routine experimentation to achieve desired characteristics as suggested by Maex et al.

Further, use of Ni-based metal *comprised of nickel alloy* and N-rich titanium nitride in the combination would provide "the nickel silicide on the gate pattern neither shorted nor cut, a pit is prevented from being formed in a boundary area between the active region and the field region, and lumping of the nickel silicide is prevented and a

silicide residue is prevented from remaining on the spacers and the field region" as claimed and well-suited with Doan et al.'s col. 6, line 62 to col. 7, line 6 "for inhibiting outgrowth of adjacent silicide contact areas which have the potential for forming short circuit paths between the silicide contact area" and preventing "pitting of the silicon substrate", Doan et al.'s col. 4, lines 64-68.

Re claims 5 and 16, in the combination, the Doan et al. reference discloses the chemical formula TiN_x where x>1 or from about 1 to 2 or 1.1 to 1.3 (col. 2, line 8, col. 3, lines 24-31, col. 6, line 8).

Re claims 6 and 17, in the combination, the Takeuchi reference discloses the thermal treatment for forming nickel silicide layer is carried out using a RTN, col. 8, line 11, not in vacuum but obviously must be in a thermal system.

Claims 2, 7-8 and 13, 18-**19**, 22-**23,** 26 and 29-30 (NOTE: Rejections of claims 29-30 have been regrouped here with their independent claims 19 and 23, respectively.) are rejected under 35 U.S.C. 103(a) as being unpatentable over the Doan et al./Takeuchi/Maex et al. combination as applied to claims **1**, 5-6 and **12**, 16-17, 27-28 and **31** above, and further in view of Catabay et al. US 6,503,840 B2, Jaiswal et al. US 6,664,166 B1 and Hill et al. US 6,775,046 B2.

The combination of Doan et al./Takeuchi/Maex et al. teaches substantially all of the instant steps of the method for fabricating a semiconductor device. Although Doan et al. teaches the transistor structure is formed using conventional technique, *metal* layer 28 for silicide and nitrogen-rich titanium nitride layer 30 are formed by sputtering

(col. 4, lines 2-4 and 35-54), and Takeuchi teaches cleaning the surface of the substrate and forming the Ni-based metal layer comprised of nickel alloy and titanium nitride layer by sputtering; however, none of the reference teaches at what temperature the Ni-based metal layer is formed, and using RF sputtering etching to remove particles from the surface of the substrate in situ with the formation of Ni-based layer and TiN layer.

Re claims 2, 13, ***19****,* 22-**23** *and* 26, the Hill et al. reference teaches

> As known, the temperature at which the target is maintained influences the composition of the alloy that is deposited on the substrate during sputtering. As example, **if** the block of metal in dish 27 is a titanium nickel alloy of 50% titanium and 50% nickel, and that target is at room temperature during the sputtering process, *the alloy deposited on the substrate will be different in composition*, namely, 48% titanium and 52% nickel. **If** the target is at 100 degrees C. during the sputtering process, then the composition of the deposited alloy will be 49% titanium and 51% nickel. And **if** the target is maintained at a temperature of 200 degrees C. during the sputtering process, the deposited alloy will be 50% titanium and 50% nickel, col. 9, lines 34-45.

Choice of temperature amongst many other variable parameters in the formation of elements would have been a matter of routine optimization because temperature is known to affect process steps and resulting device properties and would depend on the desired device density on the finished wafer and the desired device characteristics as taught by Hill at al. One of ordinary skill in the art would have been led to the recited temperature through routine experimentation to achieve desired deposition and reaction rates. It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the process of the combination with the Ni-based metal *comprised of nickel alloy* sputtering with selected temperature of about 25 to 500 ^{O}C in a thermal treatment system because the sputtering of Ni-based metal within the selected temperature range in the system would give the process of the combination with the desired metal as taught by Hill et al.

Re claims 7-8, 18-19, 22-23 and 26, the Catabay et al. reference discloses the process wherein the contaminated surface is solvent cleaned to remove residues and then RF cleaned before titanium and then titanium nitride are deposited over the surface in the same chamber (abstract). And/or the Jaiswal et al. reference discloses "a method for processing a partially fabricated semiconductor wafer … including performing a wet pre-metallization cleaning step on the surface of the wafer, performing an RF plasma sputter etching process … while maintaining unbroken vacuum conditions … and depositing a layer of metal on the surface of the wafer … a stabilization bake cycle then is performed on the wafer", col. 2, lines 50-66.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the cleaning and depositing of the combination of Doan et al. with Takeuchi and Maex et al. with the teachings of Catabay et al. and/or Jaiswal et al. because the steps of cleaning/etching and depositing of Catabay et al. and/or Jaiswal et al. would provide the process of the combination with continuous process and preventing further contamination.

Re claims 29-30, limitations are the same as in claim 19 or claim 23 plus either claim 27 or claim 28, respectively, and considered in the same manner as in claims 27-28 as followed:

The above combination teaches substantially all of the instant steps of fabricating a semiconductor device. The combination does not disclose the nickel alloy layer includes greater than 0 to about 20 % of one of the materials of Ta, Zr, Hf, Pt, Pd, V, Nb or any combination of these (excluding Ti, Co and W).

The Maex et al. reference discloses these materials as elements in a Ni alloy used to formed Ni silicide [0014] or [0019], e.g. especially [0014] discloses

> The first layer structure can also include a cobalt-nickel alloy with the nickel content varying from 0 to 100%; … Also, other metals such as Pt or Pd can be chosen as elements that are present in the first layer structure…. or the elements Pt and Pd can be added in minor amounts to the first layer structure. Also, other elements such as Au, Ir, Os, Rh, Ti, Ta, W, Mo, Cr, C, and Ge can be part of the first layer structure.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of the combination with Maex et al.'s Ni alloy containing one of Ta, Zr, Hf, Pt, Pd, V, Nb or any combination of these materials, because the Ni alloy of Maex et al. would provide the combination with materials that "can withstand thermal treatment without significant degradation" [0009].

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